Huawei is a leading telecom solutions provider. Through continuous customer-centric innovation, Huawei has established end-to-end advantages in Telecom Network Infrastructure, Application & Software, Professional Services and Devices. With comprehensive strengths in wireline, wireless and IP technologies, Huawei has gained a leading position in the All-IP convergence age. Its products and solutions have been deployed in over 100 countries and have served 45 of the world's top 50 telecom operators, as well as one third of the world's population.

Huawei Leuven R&D team develops next generation RF transceivers, supporting 4G (LTE) and 5G protocols.

Today, we're seeking team players who get things done and share a passion for bringing new wireless technologies to the rapidly growing mobile market. Now is your chance to join the engineering team and develop new, world-leading products.

Job Description

We are offering a senior layout engineer position enabling you to join the creation of the next generation mobile phone chips.

The Analog & RF IC Layout Engineer will be part of an experienced layout team. In close cooperation with his colleagues he will be in charge of the layout of high speed analog and RF circuits and he will take up a leading role in the floorplanning and optimization of the system on chip.

He is an expert user of Cadence and Mentor tool suites on nanometer RF CMOS and/or RF SOI technology.

The successful candidate will work closely with the RF designers. He/she will take into account the constraints from the designer and will go through iterations with the designer to further optimize the layout from a performance and area perspective.

RF circuit layout experience in the sub 10-Ghz range is mandatory.

The layout engineer should have a good understanding of the different circuit topologies and their constraints for the layout. implementation. Good understanding of the layout rules enables to optimize the implementation.

The senior layout engineer is also capable to perform extraction of parasitics and make the interpretation of these results in view of further optimization.

Required Education and Experience:

- Industry Degree qualified (BS or MS EE degree)
- Ample experience with the Cadence OA VirtuosoXL
- Experience with RFIC layout (GHz range) in CMOS technology
- Finfet experience is a major plus.
- Automation for layout is a plus.
- Good communication skills & team-player.
- Process oriented, ability to structure the RF layout process
- Continuous strive for improvement in circuits and process.
- Detail oriented and determined
- Relocation to Belgium, if applicable, is strongly recommended.

Location

Leuven, Belgium, on-site;

How To Apply

Send your resume to Werner.Seerden@huawei.com