DIGITAL LAY OUT (Back end) ENGINEER

Huawei is a leading telecom solutions provider. Through continuous customer-centric innovation, Huawei has established end-to-end advantages in Telecom Network Infrastructure, Application & Software, Professional Services and Devices. With comprehensive strengths in wireline, wireless and IP technologies, Huawei has gained a leading position in the All-IP convergence age. Its products and solutions have been deployed in over 100 countries and have served 45 of the world's top 50 telecom operators, as well as one third of the world's population.

Huawei Leuven R&D team develops next generation RF transceivers, supporting 4G (LTE) and 5G protocols.

Today, we're seeking team players who get things done and share a passion for bringing new wireless technologies to the rapidly growing mobile market. Now is your chance to join the engineering team and develop new, world-leading products.

Job Description

As part of its transceiver chip developments, Huawei is working on a complex mixed signal SOC in an advanced CMOS node. The successful candidate will work together with the BE implementation engineer assisting in the implementation and taking ownership of the power analysis and sign-off verification. He/she will set up the full power analysis and sign-off verification flow, execute on it, feed the information back to the other team members, analyze issues and assist in solving them.

The successful candidate needs to be a technical expert in the following areas covering the digital design flow (the items in bold are the most important ones) :

- Logic synthesis: knowledge of physical synthesis is a big plus.
- **Writing, understanding and adapting SDC based timing constraints**
- Clock tree synthesis (CTS): optimizing the clock tree is essential and often requires a mix of clock tree synthesis and (partial) manual instantiation of the clock tree for the most sensitive parts.
- Placement and routing
- **IR drop analysis**
- static timing analysis (STA) and closure
- **Signal integrity (SI) analysis and closure**

- **Structured & hierarchical layout, manual placement and routing.**
- **power analysis (static and dynamic)**
- **DRC and LVS sign-off.**

Required Education and Experience:

- Strongly Desired Education and Experience:
  - Minimum 8 years experience
  - MS in EE, Computer Engineering, or equivalent field
- Experience with digital hardware: RTL design (VHDL, Verilog), logic optimization, RTL compiler, deep sub-micron.
- Experience with (mainly Cadence) backend tools: Innovus (CTS, CPF, SDC, STA, SI, …), Redhawk, ….
- Good communication skills
- Detail oriented and determined
- Team player

Location

Leuven, Belgium

How To Apply

Send your resume to Werner.seerden@huawei.com