Huawei is a leading telecom solutions provider. Through continuous customer-centric innovation, Huawei has established end-to-end advantages in Telecom Network Infrastructure, Application & Software, Professional Services and Devices. With comprehensive strengths in wireline, wireless and IP technologies, Huawei has gained a leading position in the All-IP convergence age. Its products and solutions have been deployed in over 100 countries and have served 45 of the world's top 50 telecom operators, as well as one third of the world's population.

Huawei Leuven R&D team develops next generation RF transceivers, supporting 4G (LTE) and 5G protocols.

Today, we're seeking team players who get things done and share a passion for bringing new wireless technologies to the rapidly growing mobile market. Now is your chance to join the engineering team and develop new, world-leading products.

Job Description

As a member of the Huawei engineering team, the digital design engineer will take responsibility for the design of a single IP or the full digital toplevel of a (smaller) transceiver chip, which includes analog/RF blocks, digital blocks and in some cases SW running on the processor.

This will include the following tasks:

- Create a block level architecture based on a requirements specification
- Implement the design in verilog.
- Write small block level testbenches to debug small blocks.
- Extract from the requirements and the design specification the constraints for the design and run synthesis
- Document the design properly
- Write assertions on design/interfaces to support verification
- Assist the verification team with bringing up the verification environment and debugging the design
- Support the back-end team with timing related optimizations.
- Assist the characterization team during lab debug.

Required Education and Experience:

- MSEE or equivalent.
- Candidate should have at least 5-8 years hands-on experience in front-end digital ASIC design.
- Expert in verilog
- Experience in implementing signal processing algorithms is definitely an asset
- Experience with wireless communication chips is also an asset
- Familiar with state-of-the-art verification methodologies (Systemverilog/UVM)
- Expert in logic and physical synthesis
- Good root cause analysis and debug skills
- Good documentation skills
- Good communication skills & team-player.
- Detail oriented and dedicated

Location

Leuven, Belgium, 100 % on-site;

How To Apply

Send your resume to Werner.Seerden@huawei.com