**Huawei** is a leading telecom solutions provider. Through continuous customer-centric innovation, Huawei has established end-to-end advantages in Telecom Network Infrastructure, Application & Software, Professional Services and Devices. With comprehensive strengths in wireline, wireless and IP technologies, Huawei has gained a leading position in the All-IP convergence age. Its products and solutions have been deployed in over 100 countries and have served 45 of the world's top 50 telecom operators, as well as one third of the world's population.

**Huawei Leuven R&D** team develops next generation RF transceivers, supporting 4G (LTE) and 5G protocols.

***Today, we're seeking team players who get things done and share a passion for bringing new wireless technologies to the rapidly growing mobile market. Now is your chance to join the engineering team and develop new, world-leading products.***

## Job Description

As a member of the Huawei engineering team, the digital verification engineer will take responsibility for the verification of a single IP or the (digital) toplevel of a transceiver chip, which includes analog/RF blocks, digital blocks and SW running on the processor.

This will include the following tasks:

- Creating a verification plan based on the chip/IP definition
- Creating a testbench using industry proven verification methodologies with SystemVerilog and UVM
- Executing the verification plan through directed or constrained random verification. Full automatic regression is a must for this.
- Setting up and running gatelevel verification
- Interacting with the mixed signal verification team to support them with their activities by reusing the digital testbench for mixed signal verification.

## Required Education and Experience:

- MSEE or equivalent.
- Candidate should have at least 5-8 years hands-on experience in verification of pure digital and/or mixed signal IPs or ICs.
- Working experience in front-end design/verification.
- Expert in Systemverilog and UVM concepts and implementation.
- Capable of setting up a verification environment from scratch.
- Expert in setting up and executing gatelevel verification.
- Strong knowledge of functional and code coverage.
- Experience with formal verification is an asset
- Good root cause analysis and debug skills
- Good communication skills & team-player.
- Detail oriented and determined
- Tool/Language knowledge: System Verilog, UVM, Incisive, Scripting skills

## Location

Leuven, Belgium, 100 % on-site;

## How To Apply

Send your resume to Werner.Seerden@huawei.com